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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,920	08/29/2002	Robert T. Froebel	BUR920010211	2343

30449 7590 11/26/2004

SCHMEISER, OLSEN + WATTS
SUITE 201
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LATHAM, NY 12033

EXAMINER	
SAGAR, KRIPA	

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 11/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,920	FROEBEL ET AL.	
	Examiner	Art Unit	
	Kripa Sagar	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed 9/21/04 has been entered. Claims 1,8,13,20 are amended; new claims 21-22 are added. No new matter has been introduced by the amendment. Claims 1-22 are under consideration.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1-5, 8-11 are rejected under 35 U.S.C. 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over US Pat.5811211 to Tanaka et al.

Tanaka teaches a peripheral exposure method wherein a design (scale pattern) is printed in the peripheral region lying between the active region and the periphery of a wafer (4;28-37). It teaches passing light through an exposure apparatus [cl.8] with a lens (fig.3), a test reticle R and a reticle blind 45. Fig.4 illustrates the positioning of the blades to expose a rectangular area of the test reticle (fig.5) and thereby transfer images of the reticle onto the wafer. [cl.2]. Tanaka teaches a scale pattern (fig.5) that measures [cl.5,11] the accuracy of the blind settings (6;38-45) comprising numerical patterns (14;6-15) separated from the scale pattern [cl.3,9]. Tanaka teaches that the reticle graduations measure real distances printed on the wafer (14;16-23) and are used

to determine the settings of the reticle blind (14;24-45). The accuracy of the image printed on the wafer is the sum of all the errors (design tolerances) as shown in fig.10; this is known in the art as the error budget. Tanaka teaches (14;16-23 & 17;58-18;14) that the graduations on the scale are designed to measure the minimum error expected from the error budget [cl.4,10]. Fig.7-12 implicitly teach that the test verniers are printed in the peripheral portion of the wafer where no active areas are present.

4. Claims 1,8,13,20-22 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over US Pat.4937618 to Ayata et al.

Ayata teaches a printing method and printed wafer (fig.13) with a printed design (WPL1, WPR1) that is only within the peripheral portion of the wafer and not in the active areas 1-45. The marks (fig.15) are for coarse alignment and thus visible to the unaided eye, although machine vision (TV) may be used for alignment. The peripheral portion is implicitly outside the "outer boundary" of the active area and within the "outer boundary" (edge) of the wafer. In Fig. 5 the apparatus of the instant claims is disclosed. The reticle and blinds of the instant claims are discussed with reference to fig. 16,17.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6,7,12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of US Pat.5376482 to Hwang et al.

Tanaka teaches that the scale pattern may be incorporated into a regular reticle comprising device patterns (6;38-45) or on a separate test reticle. It teaches **[cl.7]** forming a semiconductor device (1;5-15). It does not *explicitly* teach patterning the active area and the peripheral area.

Hwang's invention is directed to a method of exposure to measure the reticle blind positioning tolerance (abstract). It teaches a mask with alignment patterns that measure the blind-setting errors (fig.2). The central portion of the mask has device patterns ("product dies") that are exposed **[cl.6,12]** along with the alignment marks (2;40-49). Hwang teaches a "plurality of space apart patterns" that are used to measure the errors in setting the blind [cl.9,10].

With reference to claim 6, Examiner notes that exposure of the "peripheral portion" of the wafer is not considered by Applicant to be critical to the invention. The specification allows for the exposure of the measurement pattern in the device area (p.9):

"For example, the present invention is not limited to printing pattern fields 51 -62 in the peripheral portion 38 of the wafer 36. Any one of the pattern fields 51 -62 can be printed within the active portion 40 of the wafer 36 by not printing at least one of the device fields 41 -49 (see FIG. 4) to create an open space adjacent a printed device field so that at least one of the pattern fields 51 -62 can be printed in the open space."

Alignment marks and focus measuring verniers are routinely exposed on scribe lines while exposing the device area.

Tanaka teaches a printed wafer **[cl.13]** with measurement pattern (fig.10). Claims **16-19** recite the same limitations as claims **3,4,6,7**. The pattern printed on the wafer is implicitly a copy [cl.**14,15]** of the pattern on the mask or a portion of it that is exposed as shown in fig.10. This is also taught by Hwang as noted above (Hwang; fig.3). Tanaka teaches that the scale patterns [cl.**20**] are easily read (6;63-7;16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Tanaka's verniers on to a device mask (as suggested by Tanaka) and simultaneously expose devices and measurement marks as taught by Hwang. Hwang teaches that this method reduces the patterning error arising from misaligned blades and increases productivity (2;55-64).

Response to Arguments

7. Applicants' arguments and remarks presented 9/21/04 have been considered but are unpersuasive.

On p.8 of the remarks it is argued that Tanaka does not teach " printing a design only within the peripheral portion of the wafer ....." and that the reference does not disclose a peripheral portion of a wafer or that it lies between the active (device) area and the outer boundary (edge) of the wafer. Tanaka's figures are explicit in defining the edge of the wafer and the region where the alignment verniers are printed with reference to the device area. Since Tanaka's invention is to blind-position calibration AND edge exposure it implicitly limits the exposure and development process to the

wafer edge away from device areas. Applicants' arguments are further unconvincing for the reason stated above and reproduce below.

The specification allows for the exposure of the measurement pattern in the device area (p.9):

"For example, the present invention is ***not limited to printing pattern fields 51 - 62 in the peripheral portion 38 of the wafer 36***. **Any one of the pattern fields 51 -62 can be printed within the active portion 40 of the wafer 36** by not printing at least one of the device fields 41 -49 (see FIG. 4) to create an open space adjacent a printed device field so that at least one of the pattern fields 51 -62 can be printed in the open space."

Alignment marks and focus measuring verniers are routinely exposed on scribe lines while exposing the device area.

On p.9, Applicants argue that Tanaka does not teach that the spacings on the design (pattern) are " equal to a design tolerance, wherein the design tolerance is a sum of a first design tolerance ....." . On p.10 they proceed to argue that there is nothing in Tanaka that teaches that a spacing between the elements is a sum of the first and second design tolerances.

This argument is not persuasive because one of ordinary skill in the art knows and Tanaka teaches that placement errors (in Tanaka's disclosure, the edge location error) comprise multiple sources (Tanaka, fig.10) such as D1 and D2; the vernier scales are deigned for measuring the minimum error budget which is the sum of the errors.

On P.11,12 Applicants' contend that the limitations of claims 6,7,13 and 12 are not disclosed in the cited references. Examiner disagrees.

Hwang clearly teaches, a pattern design for calibrating the positioning accuracy of reticle blinds, similar to the instant invention. The calibration patterns are placed next to the device fields as shown in Hwang's figures (fig.1-3). Device fields at the boundaries of the active area would meet the limitations of these claims and therefore are implicit in Hwang's teachings.

Examiner has highlighted the rejection of claims 13-20 presented in the earlier office action and restated above, for Applicants' benefit.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kripa Sagar whose telephone number is 571-272-1392. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark F Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MH/ks

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TECHNOLOGY CENTER 1700